AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A system for maintaining translation consistency in a computer which includes a single host processor designed to execute instructions of a host instruction set and software for translating instructions from a target instruction set to instructions of the host instruction set comprising:

hardware means for indicating whether a memory address to be written stores a target instruction which has been translated to at least one host instruction, the host instruction for execution by the host processor; and

software means responding to an indication that [[a]] the memory address to be written stores [[a]] the target instruction which has been translated to at least one host instruction for assuring that host instructions translated from the target instructions stored at the memory address will not be utilized once the memory address has been written.

2. (Previously Presented) A system for maintaining translation consistency as claimed in Claim 1 in which the hardware means comprises:

a look-aside buffer including a plurality of storage locations for virtual addresses and associated physical addresses, and

a storage position in each storage location of the translation look aside buffer.

3. (Previously Presented) A system for maintaining translation consistency as claimed in Claim 1 in which the software means invalidates host instructions translated from target instructions stored at the memory address.

4. (Cancelled)

5. (Previously Presented) A system for maintaining translation consistency as claimed in Claim 1 in which the software means for protecting against writing the memory address removes translations associated with the memory address.

6. (Previously Presented) A system for maintaining translation consistency as claimed in Claim 1 in which the hardware means comprises:

a look-aside buffer including a plurality of storage locations for virtual addresses and associated physical addresses, and

a storage position in each storage location of the translation look aside buffer; and

in which the software means for protecting against writing the memory address removes translations associated with the memory address.

7. (Currently Amended) A computer system comprising:

a single host processor designed to execute instructions of a host instructions set,

software for translating instructions from a target instruction set to instructions of the host instruction set,

memory for storing target instructions from a program being translated,

a translation buffer for storing host instructions translated from target instructions for execution, and

hardware means for generating an exception to write access to a target address storing a target instruction which has been translated to a host instruction.

8. (Previously Presented) A computer system as claimed in Claim 7 in which the hardware means for generating an exception comprises a translation look-aside buffer including a plurality of storage locations for virtual and physical addresses of recently accessed memory, each of the storage locations including a storage position for indicating that an instruction at a target address has been translated to a host instruction.

9. (Original) A computer system as claimed in Claim 7 further comprising software means responding to an exception to a write access to a target address storing a target instruction which has been translated to a host instruction for protecting against writing the memory address until it has been assured that translations associated with the memory address will not be utilized before being updated.

10. (Cancelled)

11. (Cancelled)

12. (Currently Amended) A method of responding to an attempt to write a memory address including a target instruction which has been translated to a host instruction for execution by a computer system including a single host processor, the method including:

marking a memory address including a target instruction which has been translated to a host instruction, the host instruction for execution by the host processor,

detecting a memory address which has been marked when an attempt is made to write to the memory address, and

responding to the detection of a memory address which has been marked by protecting a target instruction at the memory address until it has been assured that translations associated with the memory address will not be utilized before being updated.

13. (Previously Presented) A method as claimed in Claim 12 in which the marking a memory address including a target instruction which has been translated to a host instruction comprises storing an indication that a target address has been translated in a memory location of a translation look-aside buffer with a physical address of the target instruction.

14. (Cancelled)

15. (Cancelled)

16. (Cancelled)

17. (Cancelled)

18. (Currently Amended) A memory controller comprising:

an address translation buffer including a plurality of storage locations in which recently accessed virtual addresses and physical addresses represented by the virtual addresses are to be recorded,

each of the storage locations including means for indicating whether a physical address stores an instruction of a target instruction set which has been translated to an instruction of a host instruction set for execution by a computer system including a single host processor, the instruction of a host instruction set for execution by the memory controller; and

means for detecting an indication in a storage location to prevent a write access of the physical address and for indicating a subsequent operation before accessing the address.

19. (Previously Presented) A memory controller as claimed in Claim 18 in which the means for detecting an indication in a storage location to prevent a write access of the physical address and for indicating a subsequent operation before accessing the address comprises:

means for generating an exception in response to detection of an indication, and

means for responding to the exception to indicate a subsequent operation to be taken with respect to the translated host instruction before accessing the address.

20. (Original) A memory controller as claimed in Claim 18 in which the means for indicating comprises a storage position in a storage location.